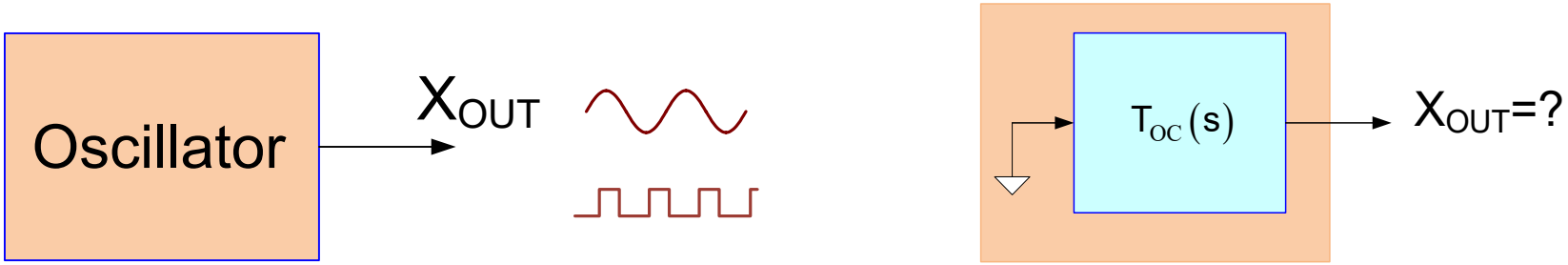
EE 508

Lecture 35

High Frequency Filters

Review from last lecture

What is the relationship, if any, between a filter and an oscillator or VCO?



- When power is applied to an oscillator, it initially behaves as a small-signal linear network
- When operating linearly, the oscillator has poles (but no zeros)
- Poles are ideally on the imaginary axis or appear as cc pairs in the RHP
- There is a wealth of literature on the design of oscillators
- Oscillators often are designed to operate at very high frequencies
- If cc poles of a filter are moved to RHP is will become an oscillator
- Can oscillators be modified to become filters?

Review from last lecture

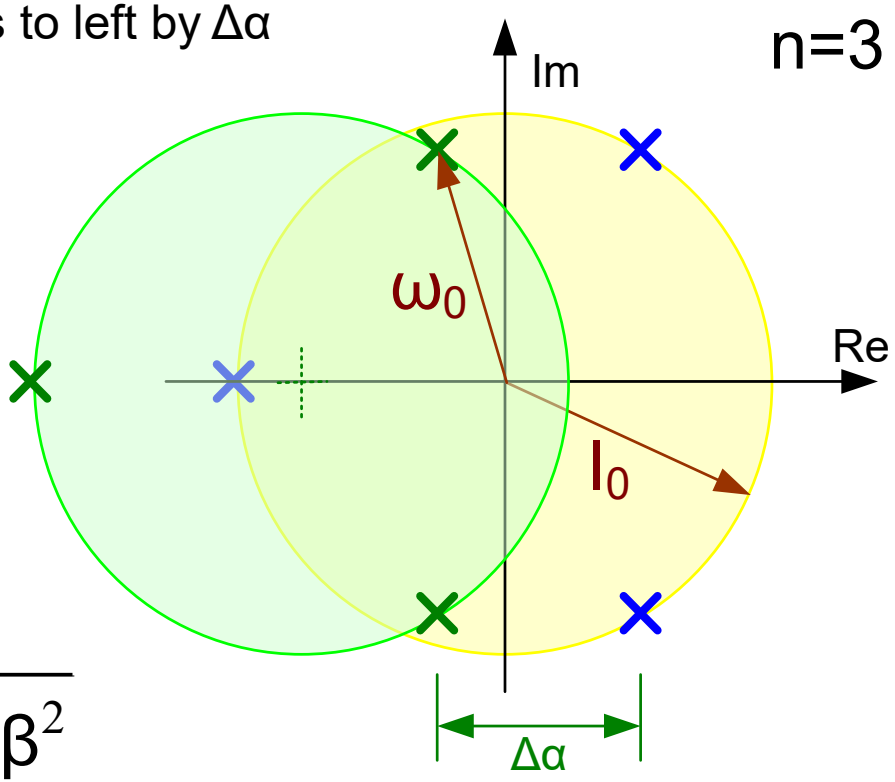
Consider the following 3-pole situation

Poles of $D(s) = s^n + I_0^n$

Consider moving all poles to left by Δα

$\beta = 0.866\ I_0$

$\alpha = 0.5\ I_0 - \Delta\alpha$

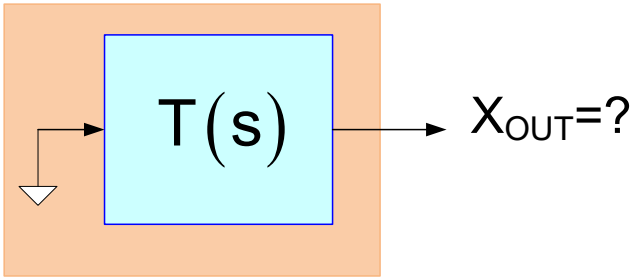


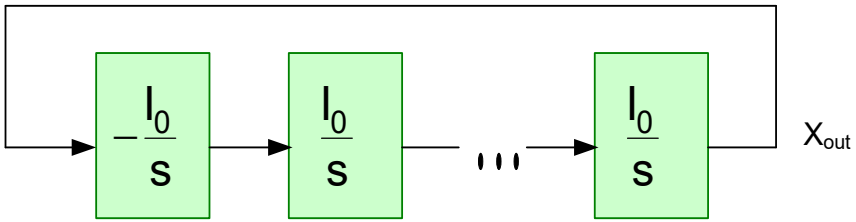
$$\omega_0 = \sqrt{(\alpha - \Delta\alpha)^2 + \beta^2}$$

So, to get a high ω_0, want β as large as possible

Review from last lecture

Consider a cascaded integrator loop comprised of n integrators





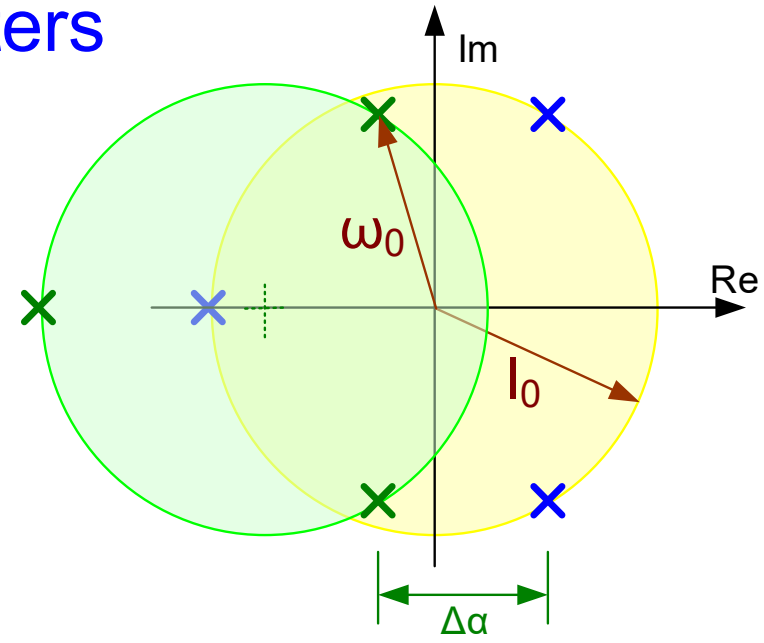
$$X_{OUT} = -\left(\frac{I_0}{s}\right)^n X_{OUT}$$

$$X_{OUT}\left(s^n + I_0^n\right) = 0$$

$$D(s) = s^n + I_0^n$$

Review from last lecture

VCO Derived Filters



- Most if not all oscillators can be modified to form a narrow-band band-pass filter

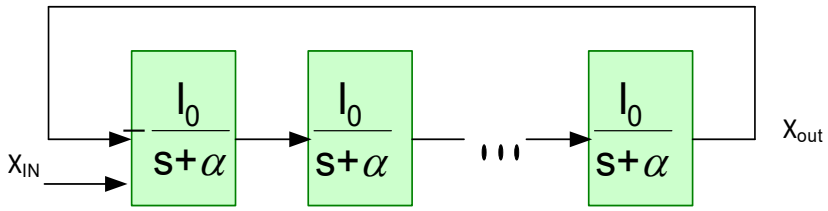
- Modification involves
- ✓ adding loss so that the pole-pair with the largest real component is in the LHP
- ✓ Introducing input to form a filter
- Can provide new filter architectures and benefit from desirable properties of the oscillator
- High frequency filters can be obtained from high frequency oscillators

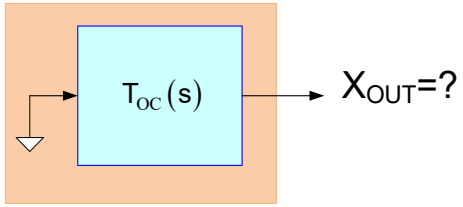
Review from last lecture

Inputs to Oscillator-Derived Filters:

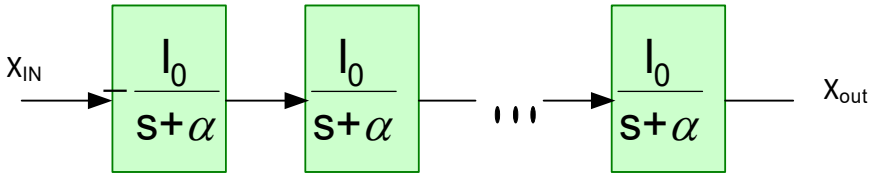
Most applicable to designing 2nd-order high frequency narrow band filters

- Add loss to delay stages
- Multiple Input Locations Often Possible
- Natural Input is Input to delay stage





- Add loss to delay stages
- Often Just Salvage Stages (drop feedback loop)
- Natural input is input to delay stage



High Frequency Filter Design

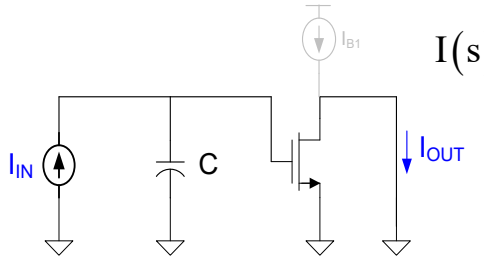
- Architecture selection is critical
- At high frequencies, simplicity of the structures is important
- Parasitic capacitances and their relationship to the time constants that can be achieved provide the ultimate limit on speed
- Will limit discussions to "inductorless" structures

High Frequency Filter Design

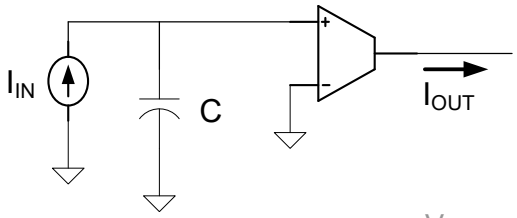
Following two methods will provide highest frequency of operation

- Degenerate VCOs
- Simple high-frequency integrator-based filters

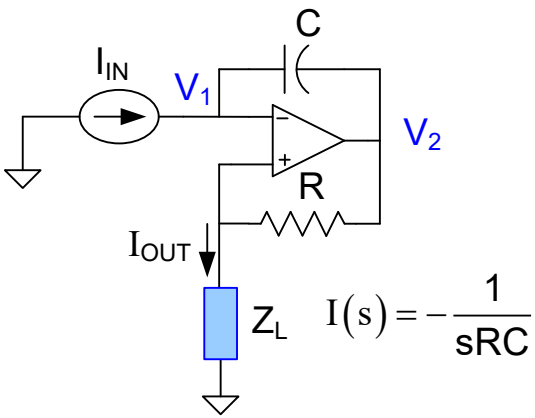
Integrator Architecture Selection



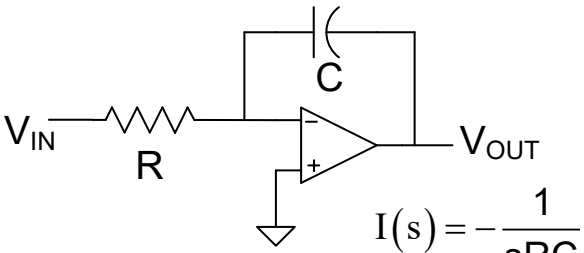
$$I(s) = -\frac{g_m}{sC}$$



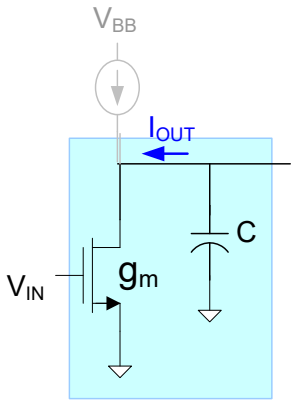
$$I(s) = \frac{g_m}{sC}$$



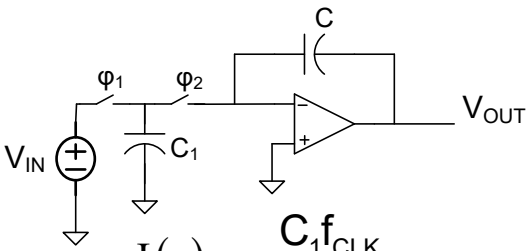
$$I(s) = -\frac{1}{sRC}$$



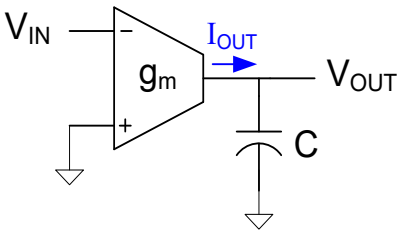
$$I(s) = -\frac{1}{sRC}$$



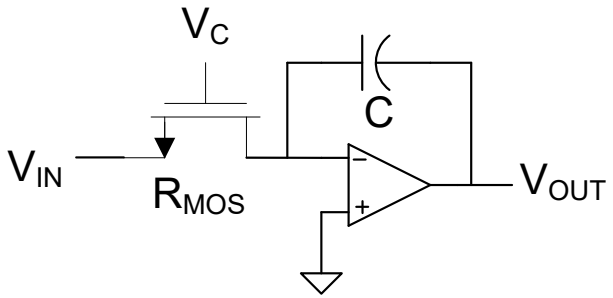
$$I(s) = -\frac{g_m}{sC}$$



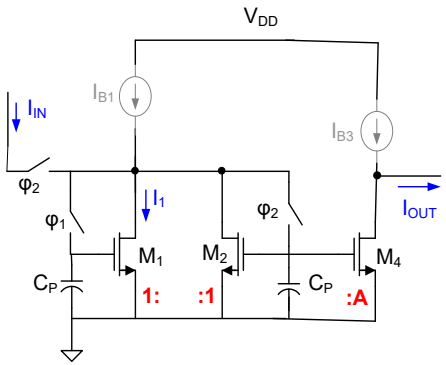
$$I(s) = -\frac{C_1 f_{CLK}}{sC}$$



$$I(s) = -\frac{g_m}{sC}$$



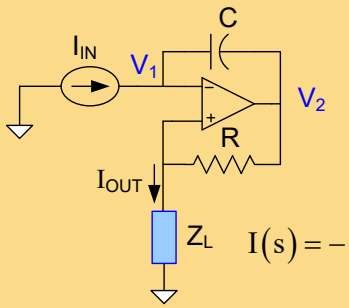
$$I(s) = -\frac{1}{sR_{MOS}C}$$



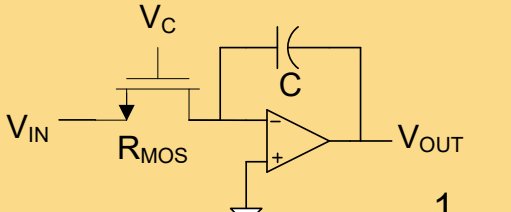
$$I(s) = -\frac{Af_{CLK}}{s}$$

Integrators for High-Speed Operation

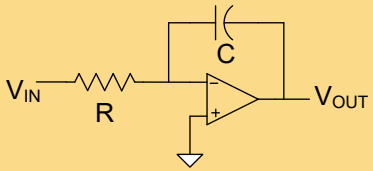
Slow



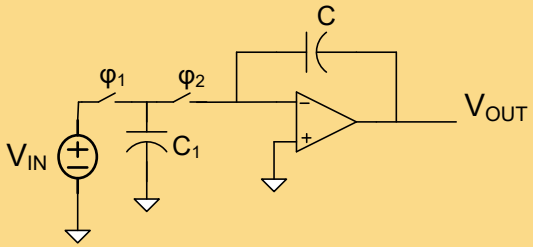
$$I(s) = -\frac{1}{sRC}$$



$$I(s) = -\frac{1}{sR_{MOS}C}$$

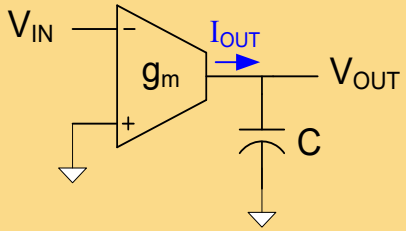


$$I(s) = -\frac{1}{sRC}$$

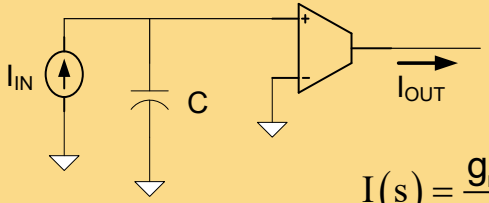


$$I(s) = -\frac{C_1 f_{CLK}}{sC}$$

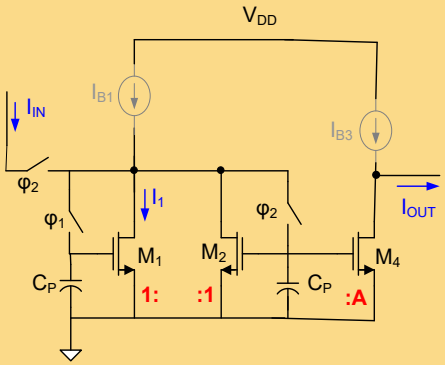
Reasonably Fast



$$I(s) = -\frac{g_m}{sC}$$

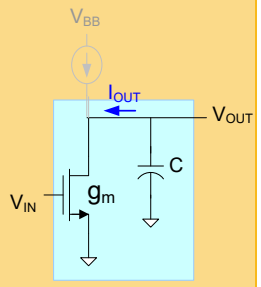


$$I(s) = \frac{g_m}{sC}$$

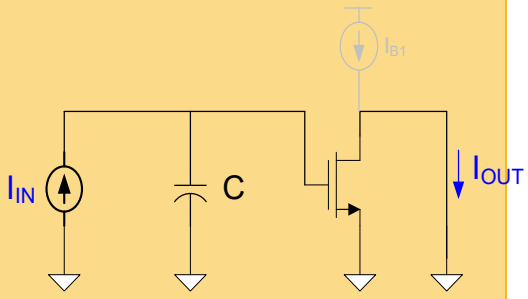


$$I(s) = -\frac{Af_{CLK}}{s}$$

Very Fast



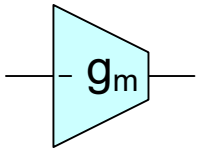
$$I(s) = -\frac{g_m}{sC}$$

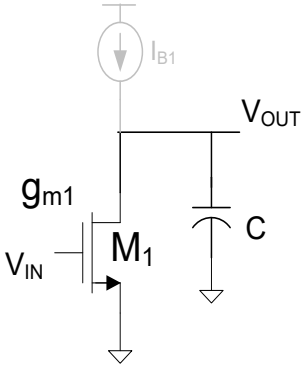


$$I(s) = -\frac{g_m}{sC}$$

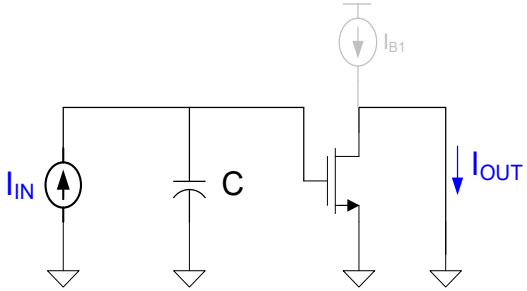
Single-ended High-Frequency TA Integrators

Structures of choice for highest-frequency of operation

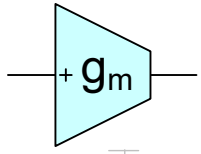


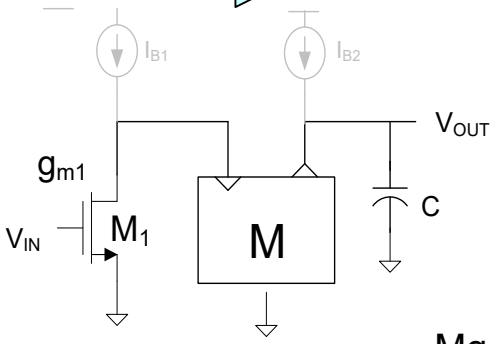


$$I(s) = -\frac{g_m}{sC}$$

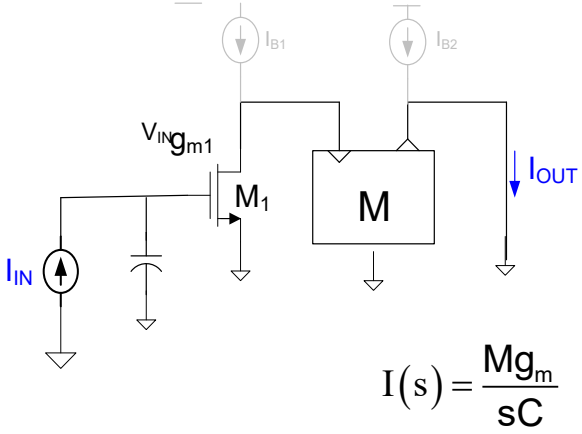


$$I(s) = -\frac{g_m}{sC}$$





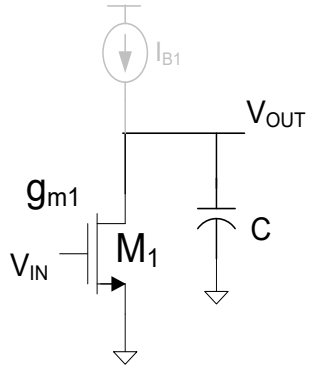
$$I(s) = \frac{Mg_m}{sC}$$



$$I(s) = \frac{Mg_m}{sC}$$

Some authors focus on voltage mode and others on current mode
But overall structures and performance appears to be identical

Single-ended High-Frequency TA Integrators



$$I(s) = -\frac{g_m}{sC} \qquad I_0 = \frac{g_m}{C}$$

Recall: ω_0 for integrator-based filters generally proportional to I_0

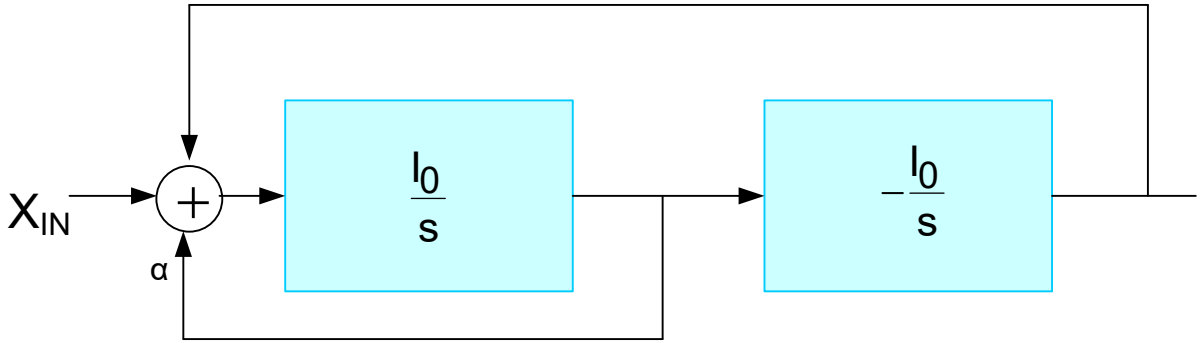
How high can I_0 be?

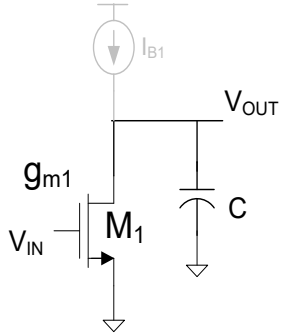
$$I_0 = \frac{W}{L}\frac{\mu C_{OX} V_{EB}}{C}$$

Looks like we can make I_0 as large as we want by making V_{EB} large, C small, L small, and W large

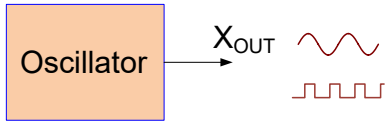
Single-ended High-Frequency TA Integrators

How high can I_0 be?

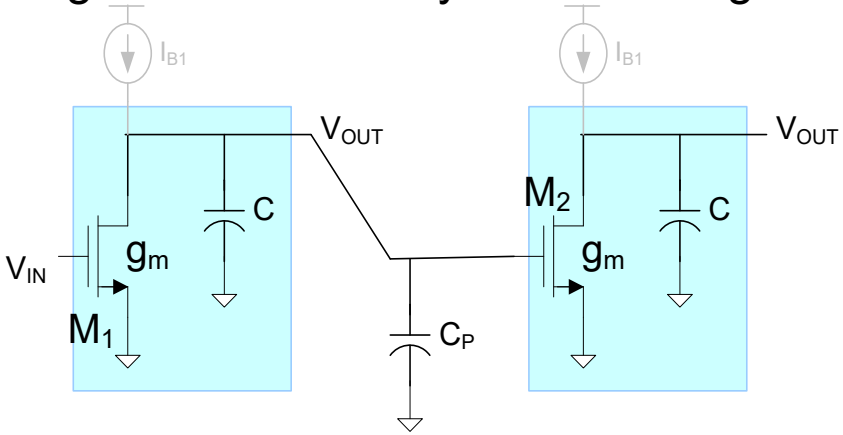




Consider a typical filter – the two integrator loop



Integrator is loaded by another integrator!



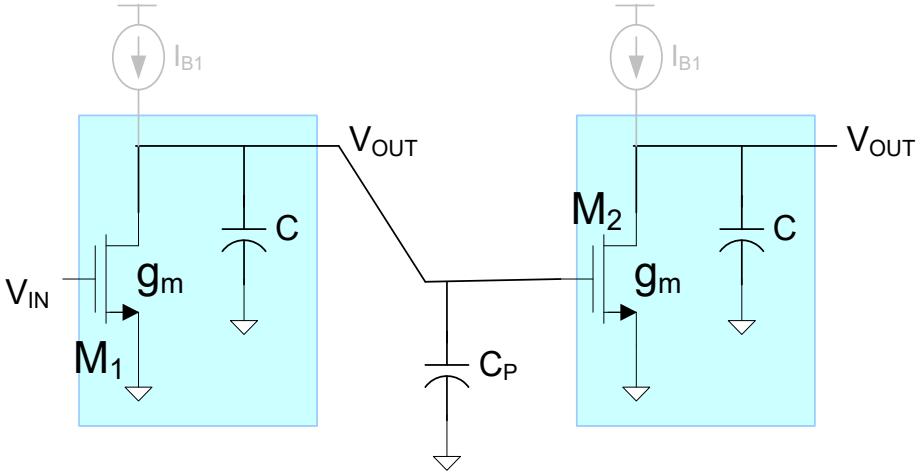
$$I_0 = \frac{W_1}{L_1}\frac{\mu C_{OX} V_{EB1}}{C + C_P + C_{OX} W_2 L_2}$$

Even if C goes to 0, I_0 is limited!

C_P is the parasitic capacitances on the output node

Single-ended High-Frequency TA Integrators

How high can I_0 be?



$$I_0 = \frac{W_1}{L_1}\frac{\mu C_{OX} V_{EB1}}{C + C_P + C_{OX} W_2 L_2}$$

Setting C to 0 and assuming C_p is small,

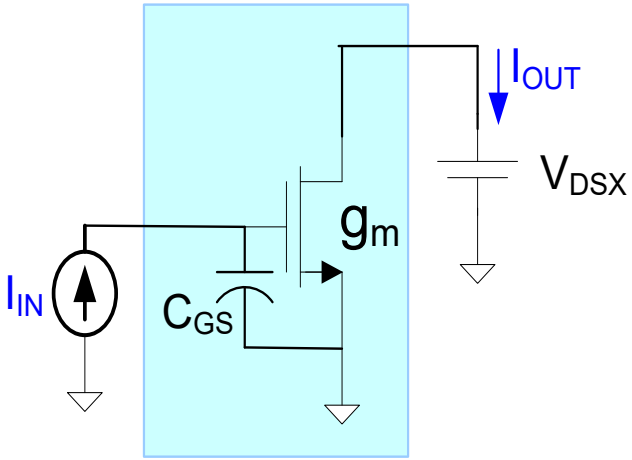
$$I_0 = W_1 / L_1 \frac{\mu C_{OX} V_{EB1}}{C_{OX} W_2 L_2}$$

$$I_0 = \frac{\mu W_1 V_{EB1}}{W_2 L_1 L_2}$$

Assuming the integrator stages are identical, it follows that

$$I_0 = \frac{\mu V_{EB1}}{L_{min}^2}$$

Transition (transit) frequency (f_T) of a process



The transit frequency of a process is the frequency where the short-circuit current gain of the common-source configuration drops to 1.

$$i_{OUT} = g_m v_{gs}$$

$$i_{IN} \cdot \frac{1}{sC_{GS}} = v_{gs}$$

$$\frac{i_{OUT}}{i_{IN}} = \frac{g_m}{sC_{GS}}$$

$$1 = \frac{g_m}{C_{GS}\omega_T}$$

$$\omega_T = \frac{g_m}{C_{GS}} = \frac{\left(\mu C_{OX}\frac{W}{L}V_{EB}\right)}{C_{OX}WL} = \frac{\mu V_{EB}}{L^2}$$

$$\omega_T = \frac{\mu V_{EB}}{L_{min}^2}$$

Journal of the Korean Physical Society, Vol. 40, No. 1, January 2002, pp. 45∼48

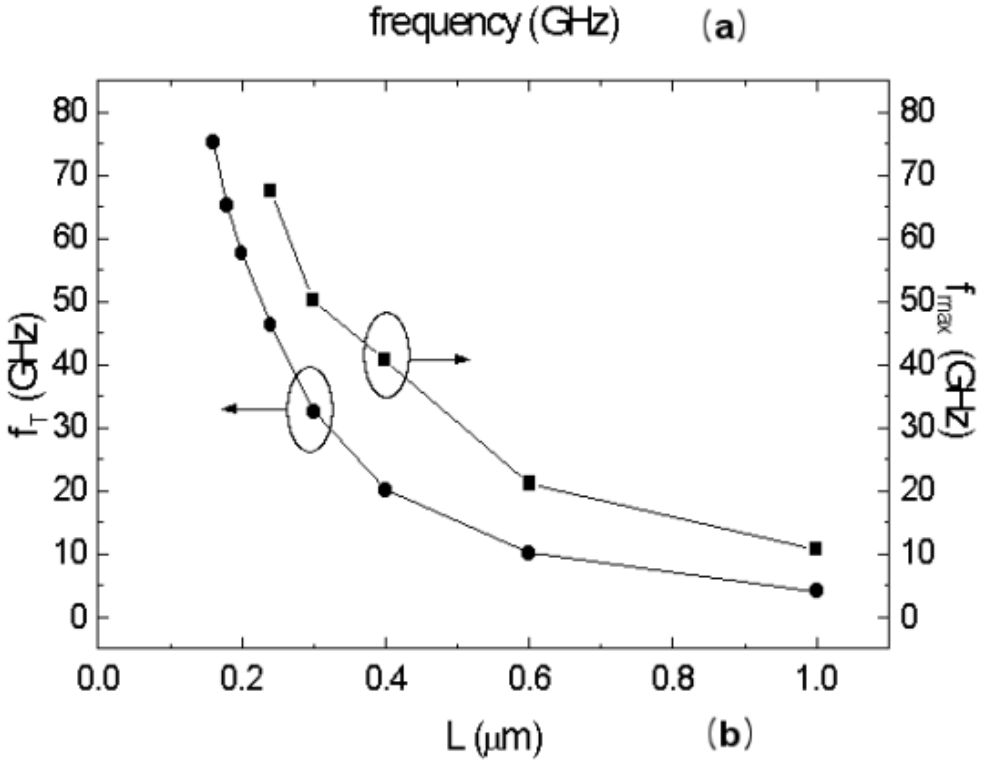
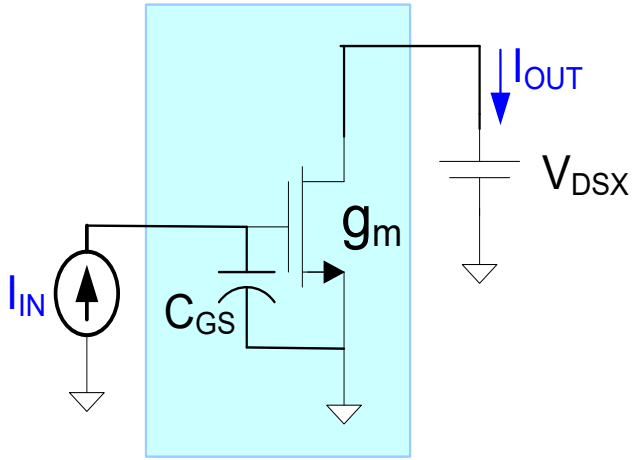


Fig. 7. (a) Maximum stable gain (MSG) and maximum available gain (MAG) for different channel lengths and (b) the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) as functions of the channel length.

Transition (transit) frequency (f_T) of a process



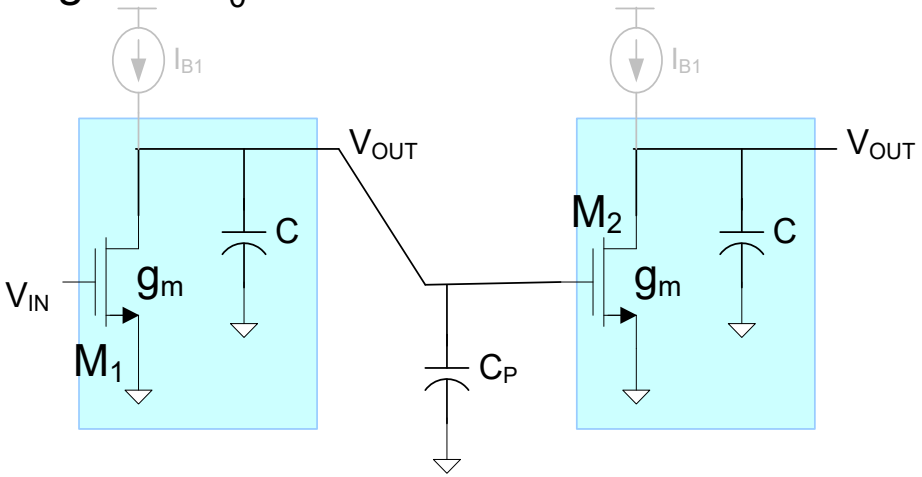
The transit frequency of a process is the frequency where the short-circuit current gain of the common-source configuration drops to 1.

$$\omega_T = \frac{\mu V_{EB}}{L_{min}^2}$$

This is dependent upon V_{EB}
Does not include effects of diffusion capacitances or overlap capacitances
f_{MAX} is another figure that characterizes the speed of a process

Single-ended High-Frequency TA Integrators

How high can I_0 be?



$$I_{0M} = \frac{\mu V_{EB1}}{L_{min}^2}$$

$$I_{0M} = \omega_T$$

(neglected C and C_P)

Speed of operation increases with V_{EB1}

V_{EB1} is limited by signal swing requirements and V_{DD}

Symmetric Signal Swing:

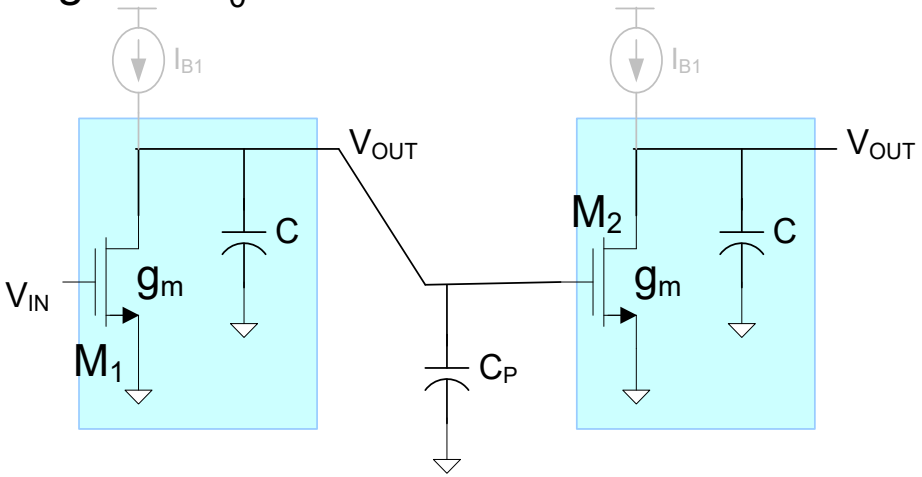
$$V_{SW} \cong \min\{V_{DD}-V_{OQ}, V_{OQ}-(V_T+100mV)\}$$

$$V_{OQ} = V_T + V_{EB}$$

$$V_{SW} \cong \min\{V_{DD}-V_T-V_{EB}, V_T+V_{EB}-(V_T+100mV)\}$$

Single-ended High-Frequency TA Integrators

How high can I_0 be?



$$I_{0M} = \frac{\mu V_{EB1}}{L_{min}^2}$$

$$I_{0M} = \omega_T$$

Speed of operation increases with V_{EB}

V_{EB} is limited by signal swing requirements and V_{DD}

Signal Swing:

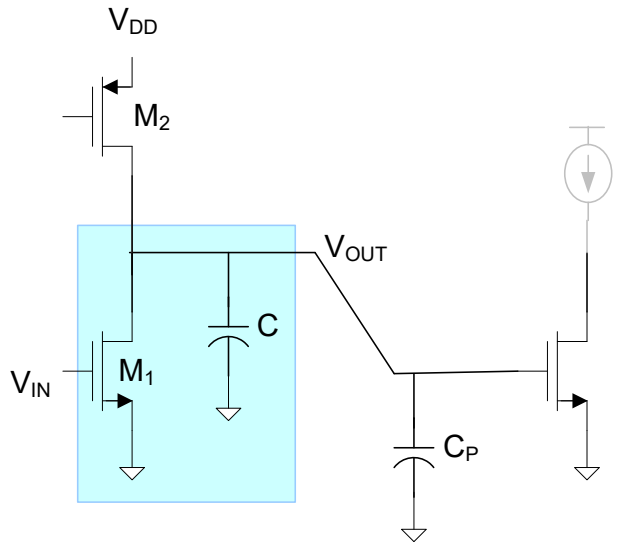
$$V_{DD} - V_T - V_{EB} = V_T + V_{EB} - (V_T + 100mV)$$

$$V_{EB} = \frac{V_{DD} + 100mV - V_T}{2}$$

$$I_{OMAX} \cong \frac{\mu(V_{DD} + 100mV - V_T)}{2L_{min}^2}$$

Single-ended High-Frequency TA Integrators

How high can I_0 be?



$$I_0 = \frac{\mu C_{OX} W_1 / L_1 V_{EB1}}{C + C_P + C_{OX} W_1 L_1}$$

Neglecting Cp and C, obtained

$$I_{0M} = \omega_T$$

$$I_{0M} = \frac{\mu V_{EB1}}{L_{min}^2}$$

Note this is independent of W_1

How much power is required to realize I_{0MAX}?

$$I_{OMAX} \cong \frac{\mu(V_{DD} + 100mV - V_T)}{2L_{min}^2}$$

$$P_{QPT} = V_{DD} I_D$$

$$P_{QPT} = V_{DD} \frac{\mu C_{OX} W_1 V_{EB1}^2}{2L_{min}}$$

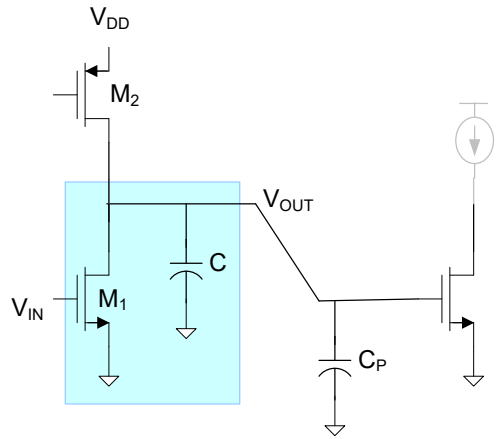
Note this is proportional to W_1

$$P_{QPT} = V_{DD} \frac{\mu C_{OX} W_{min} V_{EB1}^2}{2L_{min}} \overset{W_{min}=L_{min}}{\cong} V_{DD} \frac{\mu C_{OX} V_{EB1}^2}{2}$$

$$= V_{DD} \frac{\mu C_{OX}}{2} \left(\frac{V_{DD} + 100mV - V_T}{2} \right)^2 \overset{V_T = 0.25 V_{DD}}{\cong} V_{DD} \frac{\mu C_{OX}}{2} \left(\frac{0.75 V_{DD}}{2} \right)^2 \cong .07 \mu C_{OX} V_{DD}^3$$

Single-ended High-Frequency TA Integrators

How high can I_0 be?



$$I_0 = W_1 / L_1 \frac{\mu C_{OX} V_{EB1}}{C+C_P + C_{OX} W_1 L_1}$$

Neglecting Cp and C, obtained

$$I_{0M} = \omega_T$$

$$I_{0M} = \frac{\mu V_{EB1}}{L_{min}^2}$$

Consider again Cp and recall:

$$I_0 = \frac{W_1}{L_1} \frac{\mu C_{OX} V_{EB1}}{C+C_P + C_{OX} W_2 L_2}$$

$$I_{OMAX} \cong \frac{\mu\left(V_{DD}+100mV-V_T\right)}{2L_{min}^2}$$

C_P will modestly reduce the speed of the circuit

$$I_0 = \frac{\mu C_{OX} W_1 V_{EB1}}{L_{min} C_P + C_{OX} W_1 L_{min}^2}$$

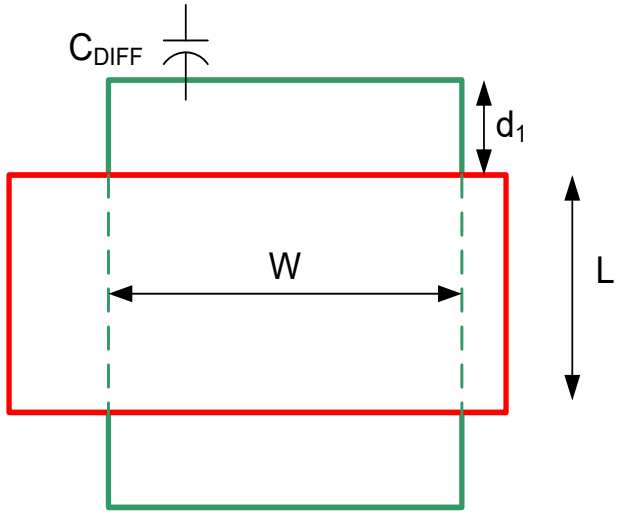
Consider the diffusion capacitances on M_1 and M_2

$$I_0 = \frac{\mu C_{OX} W_1 V_{EB1}}{L_{min}\left(C_{P1}+C_{P2}\right) + C_{OX} W_1 L_{min}^2}$$

How high can I_0 be?

The parasitic diffusion capacitances are strongly layout dependent

Consider a basic layout of a transistor



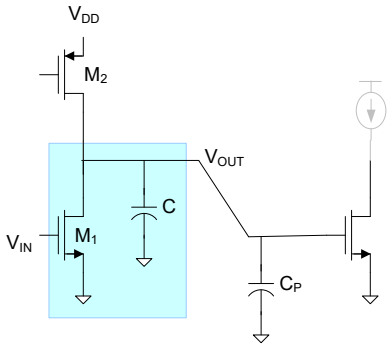
The capacitance density along the sw of the drain is usually somewhat less than that along the outer perimeters but may not easily be modeled separately

Assuming the same, drain diffusion capacitance of a transistor is given by

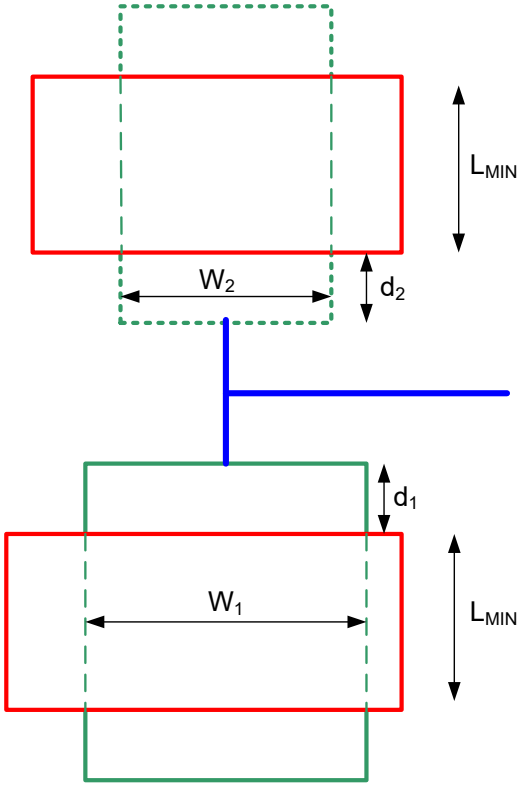
$$C_{DIFF} = C_{BOT}\left[W\, d_1\right] + C_{SW}\left[2d_1 + 2W\right]$$

C_{BOT} is the bottom diffusion capacitance density
C_{SW} is the sidwall diffusion capacitance density

How high can I_0 be?



Consider a basic layout



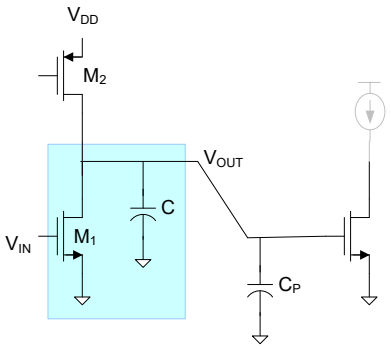
$$I_0 = \frac{\mu C_{OX} W_1 V_{EB1}}{L_{min}\left(C_{P1} + C_{P2}\right) + C_{OX} W_1 L_{min}^2}$$

$$I_0 = \frac{\mu C_{OX} W_1 V_{EB1}}{L_{min}\left(C_{BOTn}\left[W_1 d_1\right] + C_{SWn}\left[2d_1 + 2W_1\right] + C_{BOTp}\left[W_2 d_2\right] + C_{SWp}\left[2d_2 + 2W_2\right]\right) + C_{OX} W_1 L_{min}^2}$$

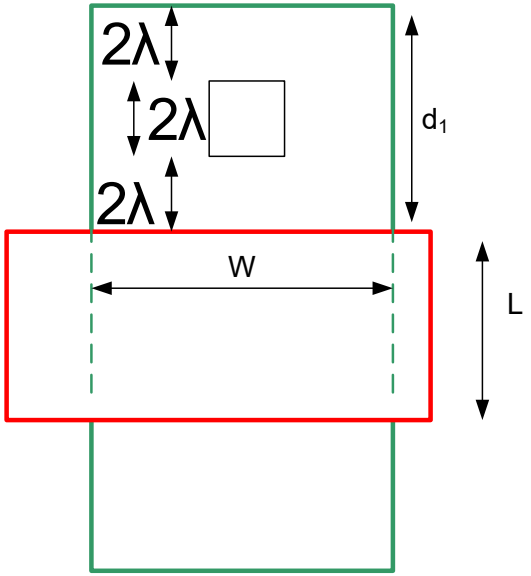
Assume $L_{MIN}=2\lambda$

$$I_0 = \frac{\mu C_{OX} W_1 V_{EB1}}{2\lambda\left(C_{BOTn}\left[W_1 d_1\right] + C_{SWn}\left[2d_1 + 2W_1\right] + C_{BOTnp}\left[W_2 d_2\right] + C_{SWp}\left[2d_2 + 2W_2\right]\right) + C_{OX} W_1 4\lambda^2}$$

How high can I_0 be?



Consider a basic layout of a transistor



$d_1 = 6\lambda$

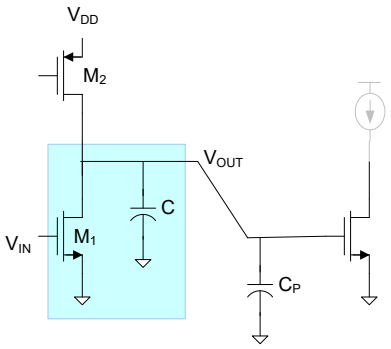
Assume $d_1 = 6\lambda$

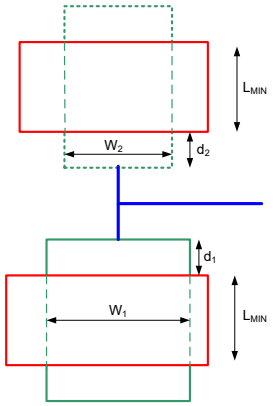
$$I_0 = \frac{\mu C_{OX} W_1 V_{EB1}}{2\lambda\left(C_{BOTn}\left[W_1 d_1\right] + C_{SWn}\left[2d_1 + 2W_1\right] + C_{BOTp}\left[W_2 d_2\right] + C_{SWp}\left[2d_2 + 2W_2\right]\right) + C_{OX} W_1 4\lambda^2}$$

$$I_0 = \frac{\mu C_{OX} W_1 V_{EB1}}{2\lambda\left(C_{BOTn}\left[W_1 6\lambda\right] + C_{SWn}\left[12\lambda + 2W_1\right] + C_{BOTp}\left[W_2 6\lambda\right] + C_{SWp}\left[12\lambda + 2W_2\right]\right) + C_{OX} W_1 4\lambda^2}$$

How high can I_0 be?

Consider a basic layout





$$I_0 = \frac{\mu_n C_{OX} W_1 V_{EB1}}{2\lambda\left(C_{BOTn}\left[W_1 6\lambda\right] + C_{SWn}\left[12\lambda + 2W_1\right] + C_{BOTp}\left[W_2 6\lambda\right] + C_{SWp}\left[12\lambda + 2W_2\right]\right) + C_{OX} W_1 4\lambda^2}$$

$$I_0 = \frac{\mu_n V_{EB1}}{4\lambda^2 + 2\lambda\left(\frac{C_{BOTn}}{C_{OX}}\left[6\lambda\right] + \frac{C_{SWn}}{C_{OX}}\left[12\frac{\lambda}{W_1} + 2\right] + \frac{C_{BOTp}}{C_{OX}}\left[\frac{W_2}{W_1}\right]\left[6\lambda\right] + \frac{C_{SWp}}{C_{OX}}\left[12\frac{\lambda}{W_1} + 2\frac{W_2}{W_1}\right]\right)}$$

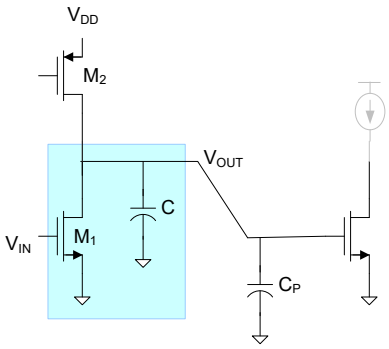
Define and assume

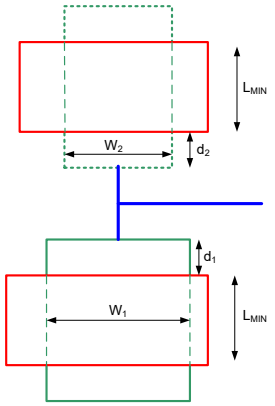
$$h_{BOT} = \frac{C_{BOTn}}{C_{OX}} = \frac{C_{BOTp}}{C_{OX}} \qquad h_{SW} = \frac{C_{SWn}}{\lambda C_{OX}} = \frac{C_{SWp}}{\lambda C_{OX}}$$

$$I_0 = \frac{\mu_n V_{EB1}}{4\lambda^2 + 2\lambda\left(h_{BOT}\left[6\lambda\right] + \lambda h_{SW}\left[12\frac{\lambda}{W_1} + 2\right] + h_{BOT}\left[\frac{W_2}{W_1}\right]\left[6\lambda\right] + \lambda h_{SW}\left[12\frac{\lambda}{W_1} + 2\frac{W_2}{W_1}\right]\right)}$$

How high can I_0 be?

Consider a basic layout





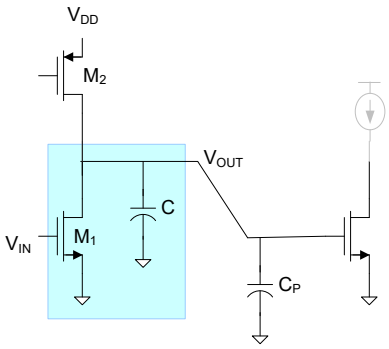
$$I_0 = \frac{\mu_n V_{EB1}}{4\lambda^2 + 2\lambda\left(h_{BOT}[6\lambda] + \lambda h_{SW}\left[12\frac{\lambda}{W_1} + 2\right] + h_{BOT}\left[\frac{W_2}{W_1}\right][6\lambda] + \lambda h_{SW}\left[12\frac{\lambda}{W_1} + 2\frac{W_2}{W_1}\right]\right)}$$

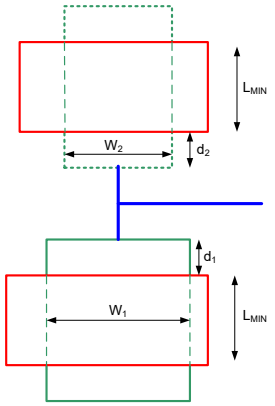
$$I_0 = \frac{\mu_n V_{EB1}}{4\lambda^2 + 4\lambda^2\left(3h_{BOT}\left[1+\frac{W_2}{W_1}\right] + h_{SW}\left[12\frac{\lambda}{W_1} + 1 + \frac{W_2}{W_1}\right]\right)}$$

$$I_0 = \frac{\frac{\mu_n V_{EB1}}{4\lambda^2}}{1+\left(3h_{BOT}\left[1+\frac{W_2}{W_1}\right] + h_{SW}\left[12\frac{\lambda}{W_1} + 1 + \frac{W_2}{W_1}\right]\right)}$$

How high can I_0 be?

Consider a basic layout





$$I_0 = \frac{\frac{\mu_n V_{EB1}}{4\lambda^2}}{1+\left(3h_{BOT}\left[1+\frac{W_2}{W_1}\right]+h_{SW}\left[12\frac{\lambda}{W_1}+1+\frac{W_2}{W_1}\right]\right)}$$

Recall

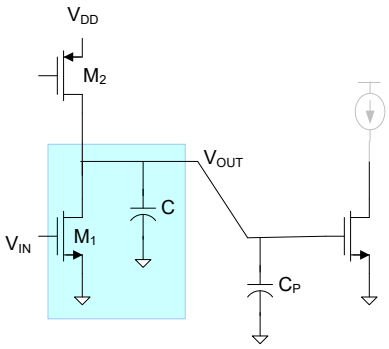
$$\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2$$

$$\omega_T = \frac{\mu_n V_{EB1}}{4\lambda^2}$$

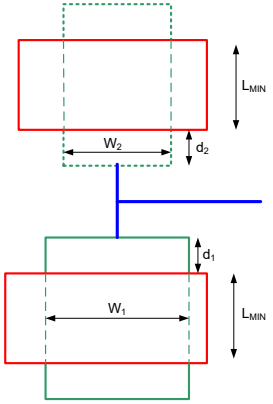
$$I_0 = \frac{\omega_T}{1+\left(3h_{BOT}\left[1+\frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+h_{SW}\left[12\frac{\lambda}{W_1}+1+\frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$

How high can I_0 be?

Consider a basic layout



$$I_0 = \frac{\omega_T}{1+\left(3h_{BOT}\left[1+\frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+h_{SW}\left[12\frac{\lambda}{W_1}+1+\frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$



Example: Consider the 0.25u TSMC CMOS Process

$C_{OX} = 5.8fF/\mu^2$

$C_{SWn} = .440fF/\mu$

$C_{SWp} = .350fF/\mu$

$C_{BOT} = 1.8fF/\mu^2$

$\frac{\mu_n}{\mu_p} = 4.1$

$\mu_n = 3.74E10$

$\lambda = 0.125\mu$

$$h_{BOT} = \frac{C_{BOTn}}{C_{OX}} = \frac{C_{BOTp}}{C_{OX}}$$

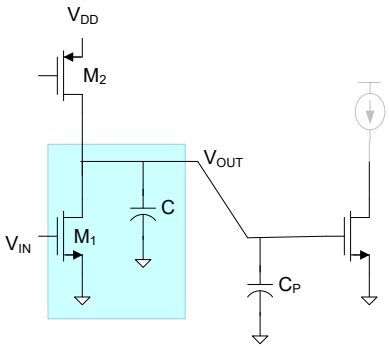
$h_{BOT} = 0.31$

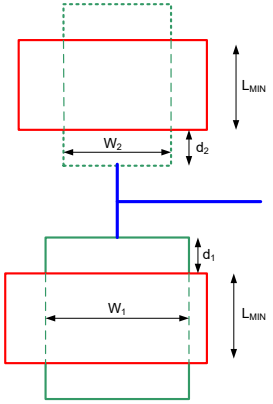
$$h_{SW} = \frac{C_{SWn}}{\lambda C_{OX}} = \frac{C_{SWp}}{\lambda C_{OX}}$$

$h_{SW} = 0.61$

How high can I_0 be?

Consider a basic layout





$$I_0 = \frac{\omega_T}{1+\left(3h_{BOT}\left[1+\frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+h_{SW}\left[12\frac{\lambda}{W_1}+1+\frac{\mu_n}{\mu_p}\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$

Example: Consider the 0.25u TSMC CMOS Process

$$I_0 = \frac{\omega_T}{1+\left(3\bullet 0.31\left[1+4.1\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+0.61\left[12\frac{0.125}{W_1}+1+4.1\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$

$$I_0 = \frac{\omega_T}{1+\left(0.931\left[1+4.1\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+0.61\left[\frac{1.5}{W_1}+1+4.1\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$

GATE term

BOT term

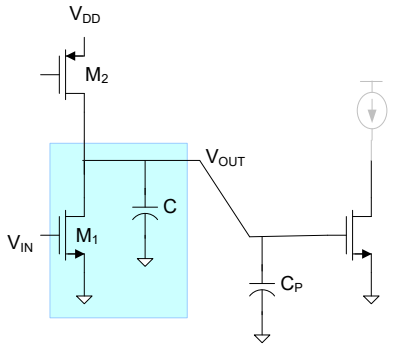
SW term

$h_{BOT} = 0.31$

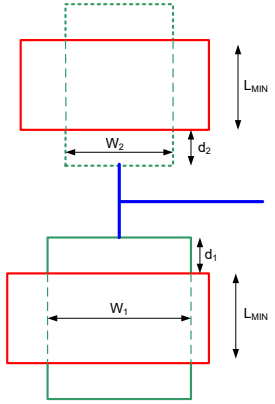
$h_{SW} = 0.61$

$\frac{\mu_n}{\mu_p} = 4.1$

How high can I_0 be?



Consider a basic layout



Example: Consider the 0.25u TSMC CMOS Process

$$I_0 = \frac{\omega_T}{1+\left(0.93\left[1+4.1\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]+0.61\left[\frac{1.5}{W_1}+1+4.1\left(\frac{V_{EB1}}{V_{EB2}}\right)^2\right]\right)}$$

GATE term

BOT term

SW term

If W_1=1.5u and V_{EB1}=V_{EB2}

$$I_0 = \frac{\omega_T}{1+(4.73+4.03)} = .102\omega_T$$

- Designer has control of V_{EB1} andV_{EB2}
- The diffusion capacitance term can dominate the C_{GS} term
- The SW capacitance can be the biggest contributor to the speed limitations
- A factor of 10 or even much more reduction in speed is possible due to the diffusion parasitics and layout
- Maximizing W_1 will minimize I_0 but power will get very large for marginal improvement in speed

Stay Safe and Stay Healthy !

End of Lecture 35